CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit, comprising:

a plurality of first circuit blocks;

a plurality of switching transistors for connecting power supply terminals of said first circuit blocks to a power supply line, respectively;

an internal power supply line for connecting to each other said power supply terminals of said first circuit blocks operating at different timings among said first circuit blocks; and

a power supply control circuit for simultaneously turning on said switching transistors connected to said internal power supply line, in response to operation(s) of at least any one of said first circuit blocks connected to said internal power supply line.

2. The semiconductor integrated circuit according to claim 1, wherein threshold voltages of said switching transistors are higher than the threshold voltages of internal transistors included in said first circuit blocks.

3. The semiconductor integrated circuit according to claim 1, wherein:

said first circuit blocks each includes a plurality of internal transistors; and

said power supply line is connected to source electrodes of said internal transistors turned off during a standby state of the semiconductor integrated circuit via said internal power supply line and said switching transistors, in each of said first circuit blocks.

4. The semiconductor integrated circuit according to claim 1, wherein

said switching transistors and said first circuit blocks are dispersedly arranged.

5. The semiconductor integrated circuit according to claim 4, wherein:

said switching transistors and said first circuit blocks are arranged in a matrix form with intervals in between; and

said internal power supply line connects to each other said power supply terminals of said part of said first circuit blocks, the connection done along a line with a smaller number of first circuit blocks operating simultaneously.

6. The semiconductor integrated circuit according to claim 4, wherein:

said switching transistors and said first circuit blocks are arranged in a matrix form with intervals in between;

said first circuit blocks aligned in one direction operate simultaneously;

said first circuit blocks aligned in a direction perpendicular to said one direction operate at different timings; and

said internal power supply line connects said power supply terminals of said first circuit blocks to each other, the first circuit blocks being aligned in said direction perpendicular to said one direction.

7. The semiconductor integrated circuit according to claim 4, comprising:

a plurality of rectangular memory cell arrays arranged in a matrix form with intervals in between, each having memory cells each connected to a word line and a bit line;

said first circuit blocks arranged in areas adjacent to four corners of said memory cell arrays, each including array control circuits for controlling said memory cell arrays and said switching transistors; and

said internal power supply line connecting power supply terminals of said array control circuits to each other, which are aligned in one of wiring directions of said word line and said bit line.

8. The semiconductor integrated circuit according to claim 7, wherein

said array control circuits connected by said internal power supply line are column control circuits for inputting/outputting data transmitted to said bit line.

9. The semiconductor integrated circuit according to claim 7, wherein

said array control circuits connected by said internal power supply line are row control circuits for selecting said word line.

10. The semiconductor integrated circuit according to claim 7, wherein

each of said array control circuits connected by said internal power supply line includes a column control circuit for inputting/outputting data transmitted to said bit line and a row control circuit for selecting said word line.

11. The semiconductor integrated circuit according to claim 7, wherein

each of said array control circuits connected by said internal power supply line includes a read control circuit operating during a read operation and a write control circuit operating during a write operation.

12. The semiconductor integrated circuit according to claim 4, comprising

a plurality of memory cell arrays each having memory cells each connected to a word line and a bit line, wherein

each of said first circuit blocks connected by said internal power supply line includes a read control circuit operating during a read operation and a write control circuit operating during a write operation.

13. The semiconductor integrated circuit according to claim 4, further comprising:

second circuit blocks respectively arranged between said first circuit blocks connected by said internal power supply line, said second circuit blocks operating at different timings from said first circuit blocks; and

power supply lines of said second circuit blocks connected to said internal power supply line.

14. The semiconductor integrated circuit according to claim 13, wherein:

said second circuit blocks each includes a plurality of internal transistors; and

said power supply line is connected to source electrodes of said internal transistors

turned off during a standby state of the semiconductor integrated circuit via said internal power supply line and said switching transistors, in each of said second circuit blocks.

15. The semiconductor integrated circuit according to claim 13, wherein

said second circuit blocks operate at different timings from each other.

16. The semiconductor integrated circuit according to claim 13, comprising

a plurality of memory cell arrays each having memory cells each connected to a word line and a bit line, wherein

said first circuit blocks connected by said internal power supply line are column control circuits for inputting/outputting data transmitted to said bit line; and

said second circuit blocks are row control circuits for selecting said word line.